

DEVELOPING AND TESTING ELECTRONIC CONTROL UNITS FOR ELECTRIC DRIVES

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Electric drives have many advantages over other types of drives and can be used in a wide range of applications. They have therefore been increasingly used in vehicles over the last years, but they will also play an important role in aircraft in the future. Because electronic control unit (ECU) signals are dynamic, developing the ECUs and power electronics for electric drives poses special requirements for development and testing tools. Particularly when electric drives are simulated, there are scenarios that require the simultaneous computation of complex simulation models in real time and highly precise measurement of the ECU signals. This paper presents the current state of the technology for developing and testing electric drive ECUs, mainly based on automotive applications. It particularly highlights the challenges of hardware-in-the-loop tests of these ECUs.

Nomenclature

<i>AC</i>	=	alternating current
<i>BLDC</i>	=	brushless DC electric motor
<i>DC</i>	=	direct current
<i>ECU</i>	=	electronic control unit
<i>FPGA</i>	=	field-programmable gate array
<i>HIL</i>	=	hardware-in-the-loop
<i>I/O</i>	=	input/output
<i>LVDT</i>	=	linear variable differential transformer
<i>MEA</i>	=	more electric aircraft
<i>PSM</i>	=	permanent magnet synchronous motor
<i>RCP</i>	=	rapid control prototyping

I. Introduction

OVER the last few years, electric drives have become more widespread, not only in vehicles but also in the fields of drive and automation technology. In the future, electric drives will be used increasingly in aircraft. The term 'more electrical aircraft' (MEA) has been coined to describe this trend toward replacing pneumatics and hydraulics for an aircraft's secondary power needs with power from electric generators. The objective is to produce more eco-friendly and economical aircraft.

In automotive applications, electric drives are already being integrated into fundamental, complex and safety-related vehicle functions. Some well-known examples are hybrid or purely electric vehicle drives; others are electric steering systems, electric brake systems, and auxiliary aggregates (oil pumps, water pumps, etc.).

This paper describes today's state-of-the-art technology for developing and testing electric drives, mainly based on automotive applications. Following on from this, the challenges that electric drives pose for hardware-in-the-loop

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(HIL) tests of electric drive ECUs will be described. These do not depend so much on the application (automotive, aerospace, etc.) and are similar across different applications.

In Section II an overview is given about the use cases for embedded system tool-chain (i.e. rapid control prototyping and hardware-in-the-loop simulation in actuator development. In addition a high-level overview about electric actuator technology and motor control technology is given.

Section III the outline of rapid control prototyping and its challenges is given.

In section IV the challenges that HIL testing faces and solutions for these challenges are provided, which are presented in more detail in the following sections. Section V focuses on the two most used simulation types, processor-based simulation and FPGA-based simulation. Based on these sections, Section VI describes HIL simulation at signal level, electronic power level, and mechanical level.

II. Use Cases for Embedded System Tool-Chain in Actuator Development

Rapid Controls Prototyping (RCP) and Hardware-In-the-Loop (HIL) technologies for simulation of controller hardware and software, as well as simulation of actuator including motor and overall system are commonly used in development of actuation technology. These technologies can be applied not only for software development and testing but also for running rigorous testing of hardware components.

Use of Rapid Controls Prototyping platform in development for controller simulation could use one of more components of either processor or FPGA (i.e. computation platform), and power electronics. On the other hand with HIL application, the development platform could include simulation of the entire system, or subsystem all the way up to the power electronics of controller unit. Typical use cases for RCP and HIL development systems are listed in Table 1. How the use of RCP and HIL systems is related to the interfaces of electric drives is shown in Figure 1. This will be discussed in more detail in section IV with regard to HIL systems.

A. Electric Actuators

The two main types of electric actuators are linear and rotary actuators. Linear actuators are further classified as either direct drive or geared drive, depending on the coupling with the end effector. The types of sensors used in the system particularly for motion sensing vary from LVDT to resolver, depending on the type of actuator. The other components of the actuator – motor and power electronics will remain the same across the actuator type but will of course appropriate for the power level of the system.

Various types of electric motors (induction, DC, brushless DC (BLDC), permanent magnet synchronous motors) are used in these actuator applications. AC induction motors are commonly used for high power applications requiring higher torque and speed, whereas DC motors are of the used for higher precision, lower power applications. In both cases power inverter based controls can be applied, even though the actual techniques vary depending on the motor and application: only speed control vs. speed, power and position control may.

Table 1. Use cases for RCP and HIL tests.

Use Case	Type of Development System
Actuator Acceptance Test	RCP
Controller and Actuator Prototyping	RCP
Actuator Simulation	HIL
Actuator Simulation + System Simulation	HIL
System Integration Testing	HIL

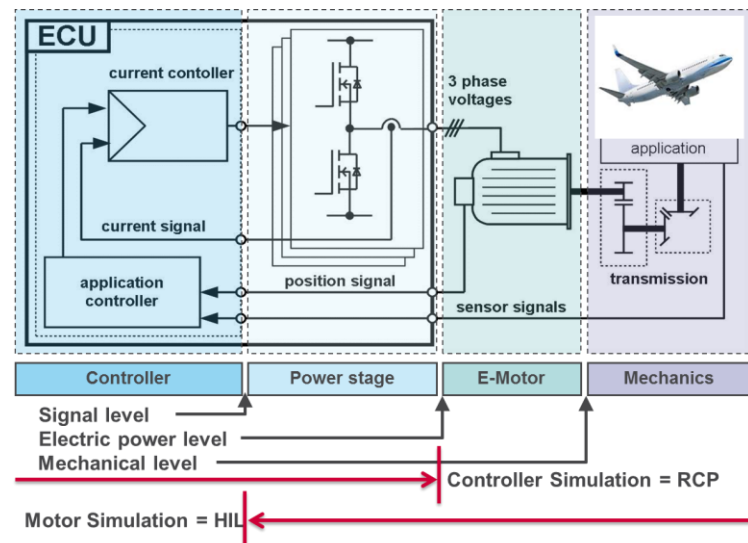


Figure 1. RCP and HIL simulation for motorized actuator systems.

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The diagram illustrates a PSM-based speed feedback control system. The reference speed n^* is compared with the actual speed n to produce a speed error signal. This error is processed by a speed controller to generate a reference d-axis current $i_{sd}^* = 0A$. The reference d-axis current is then compared with the actual d-axis current i_{sd} to produce a d-axis current error, which is fed into a d-axis current controller. The reference q-axis current i_{sq}^* is compared with the actual q-axis current i_{sq} to produce a q-axis current error, which is fed into a q-axis current controller. The outputs of the d and q current controllers are summed and fed into a decoupling block. The decoupling block outputs i_{sd} and i_{sq} to a d-q to a-b-c converter block. The outputs of this block are fed into a Modulator, which generates the reference voltages u_{sd}^* and u_{sq}^* . These reference voltages are compared with the actual voltages u_{sd} and u_{sq} to produce voltage errors, which are fed into a voltage controller. The outputs of the voltage controller are fed into a PSM (Pulse Width Modulation) block, which generates the motor voltages u_a , u_b , and u_c . The motor voltages are applied to the motor, which is represented by a three-phase motor model. The motor outputs the actual speed n and the actual d-axis current i_{sd} and q-axis current i_{sq} . The actual speed n is fed back to the speed error calculation. The actual d-axis current i_{sd} and q-axis current i_{sq} are fed back to the current error calculations. The actual motor voltages u_a , u_b , and u_c are fed back to the voltage error calculations. The motor is also connected to a PSM (Pulse Width Modulation) block, which generates the motor voltages u_a , u_b , and u_c . The motor is represented by a three-phase motor model. The motor outputs the actual speed n and the actual d-axis current i_{sd} and q-axis current i_{sq} . The actual speed n is fed back to the speed error calculation. The actual d-axis current i_{sd} and q-axis current i_{sq} are fed back to the current error calculations. The actual motor voltages u_a , u_b , and u_c are fed back to the voltage error calculations.

In case of permanent magnet synchronous motors (PSM) motors, additional sensors for current and voltage measurement are required (ref. Figure 3).

The two main implications for RCP and HIL systems are the type of I/O and computation power. First, Resolver, LVDT or encoder need specific type I/O channels with appropriate processing for speed or position. Secondly, the PWM control signals for power electronics typically range from 5-20 kHz which requires high speed computation of control signals and may require use of FPGA hardware, This is a bigger challenge for the HIL side where the computation of motor model has to be at least twice the speed of the control loop, requiring very fast computations.

Their advantages of mechatronic integration of electric motors are accompanied by a higher workload for integrating the additional control algorithms into the respective controller. The result is a more complex controller software, which usually leads to increased development times. This drawback can be countered by using model-based design along with rapid control prototyping (RCP) to accelerate design iterations of the control algorithm on the real object. Figure 5 visualizes the model-based development workflow for rapid control prototyping together with the applied HW and SW tools.

The diagram illustrates the system architecture, showing the interaction between the RS485 drivers, the FPGA (Fast Task - Motor Control), and the Processor + IO (Slow Task). The RS485 drivers manage external communication, while the FPGA handles real-time motor control tasks. The Processor manages high-level control and communication. A Memory Interface connects the FPGA and Processor. The diagram details the flow of data and control signals between these components, including input/output signals, settings, SPI data, and various control signals like 'input value adjust', 'output value adjust', 'extra-Digin', 'Digin-Hall', 'Digin-Inc', and 'DigOut (TTL value)'.

- Powerful system architecture
- Flexible I/O interfaces
- Dynamic power stages

It is crucial to meet these requirements, since developers need to concentrate completely on the function development and should not have to worry about the performance of the prototyping hardware. Ideally, you can optimize your function designs both on the test bench and in the actual vehicle or industrial drive system

until they meet the requirements – all without having to do any programming.

In addition, an intuitive software environment is required, in order to run development cycles as efficient as possible. Figure 5 visualizes this based on the tools Simulink and ControlDesk. The latter is a standard universal experiment and visualization software for electronic control unit (ECU) development.

An example for the high demands on rapid control prototyping systems are the execution speeds of control loops. For precise control of highly dynamic systems, the control loops are desired to run at very high execution speeds of over 100 kHz. Advanced RCP systems (e.g. MicroAutoBox II), augment the processor based computation with special FPGA based computation and sensor interface capabilities to meet with these requirements.

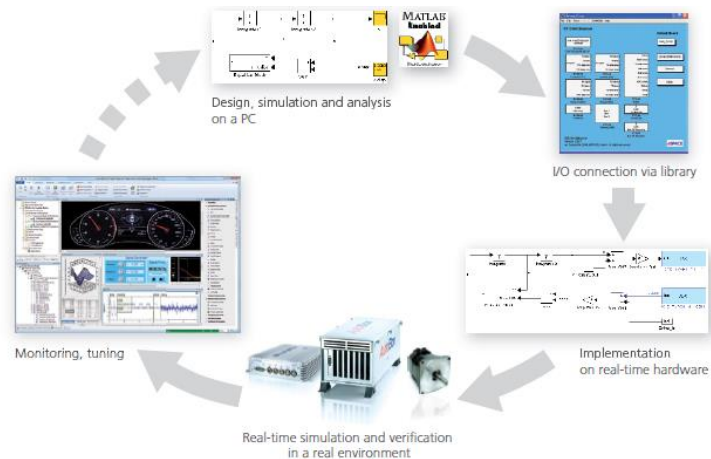


Figure 5. Model-based design workflow for rapid control prototyping

IV. Hardware-in-the-Loop Simulation for Electric Drives

Hardware-in-the-loop (HIL) simulation is an integral and reliable part of the development process. Hardware-in-the-loop simulation is used for testing ECU functions, for system integration, and for testing ECU communication. The environment of the ECUs to be tested is simulated in real time (Figure 6). The environment can consist of interacting system components such as sensors and actuators, other subsystems or complete systems, and the aircraft or vehicle environment.

The main advantages of HIL tests are reproducibility, systematic and automated testing also outside of safe system states, and the traceability of problems observed in the field. This makes it possible to conduct tests efficiently (time, costs) and as early as possible in the development process. The trend to test with virtual (i.e., simulated) ECUs that are later replaced with real ECUs highlights the importance of early testing (Ref. 2).

A general challenge for the HIL testing of electric drive ECUs arises from the fundamental difference between electric drives and other drives: The ECU has to control the drive power directly. This is unlike ECUs for other types of drives, which regulate the thermodynamic or hydraulic power via actuators (such as valves) that require comparatively little power.

Figure 1 is a schematic of an electric drive, including the motor ECU that is to be tested via HIL simulation. The motor ECU can be divided into a controller and a power stage. On the controller, the control algorithms (usually for field-oriented control) are executed, such as a secondary current controller and a primary controller for motor speed or torque. The controllers use their sensor values to calculate the necessary actuating values as multiphase PWM signals. The power stage (usually a B6 bridge) reinforces the signals. The three-phase motor is connected to the power stage.

To test a motor ECU via HIL simulation, it has to be determined which drive components enter the HIL test as real components and which are to be simulated.

There are three interfaces that can be used to connect the real and simulated components:

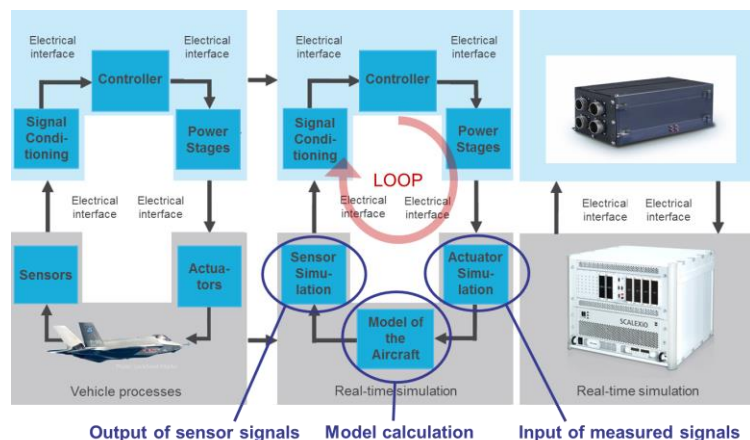


Figure 6. Hardware-in-the-loop simulation.

- Interface between controller and power stage
- ECU connector as interface
- Mechanical interface of the drive

A. Simulation at Signal-Level

Simulation at signal level means that the interface between the controller and the power stage is used for the HIL test. Here, the power stage, the current signal, the electric motor, and the mechanical drive components are simulated.

Simulation at signal level is used because it is cost-efficient and relatively easy to implement. During simulation at signal level, the high output voltages and output currents of the power stage do not have to be handled, only the signals to control them. A drawback of simulation at signal level is that the power stage is not tested.

A prerequisite for simulation at signal level is that the interface between the controller and the power stage can be accessed for the HIL test. In many electric drive ECUs, this interface is not accessible from the outside. In this case, HIL tests cannot be carried out with the production ECU, only with an open ECU or one that is modified for testing.

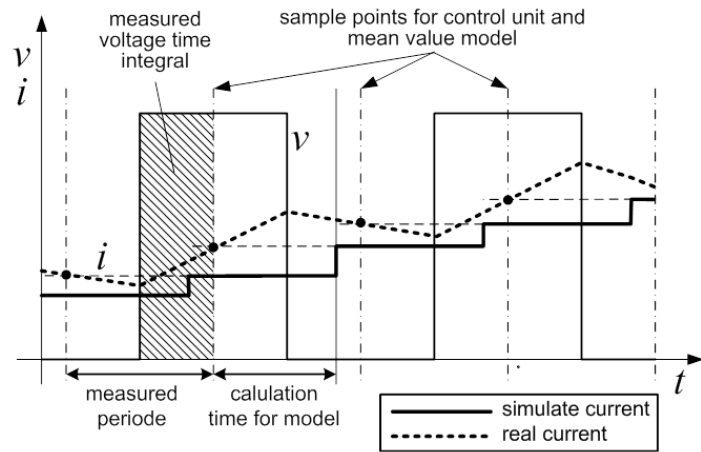
C. Simulation at Electric Power Level

If the ECU connector is used as an interface for the HIL test, the simulation is performed at power level. Here, the electric motor and the mechanical drive components are simulated. The real currents of the electronic power stage are generated by electronic load emulation at the electronic power level. This emulates the motor's load behavior.

Typical advantages of simulation at power level are that the real power electronics are included in the test, that the ECU connector is used as the interface and that, therefore, unaltered production ECUs can be tested and error states can be simulated.

To use these advantages, it is necessary to work with high voltages and currents and to use devices for load emulation. This makes tests at the electronic power level more expensive than tests at signal level and workplace safety has to be ensured.

In the automotive industry, simulation at power level has become the standard for HIL tests of ECUs for small motors. Some application examples include HIL tests of the ECUs for electric power steering (EPS), fuel pumps, and pumps for selective catalytic reduction (SCR), a means of exhaust gas aftertreatment in commercial vehicles. There is also a growing interest in using HIL tests for the ECUs of electric drive motors.



D. Simulation at Mechanical Level

In addition to the procedures described above, mechanical drive interfaces are used for HIL tests. Such a simulation at the mechanical level requires a completely mechanical test bench with the electric motor that is controlled by the ECU. Another motor is needed as a load machine whose load torque is controlled dynamically via the real-time simulation.

The advantages of this approach are the low modelling effort and the inclusion of the controlled electric motor in the HIL test. In addition to the electric motor, simulations at the mechanical level can also include the

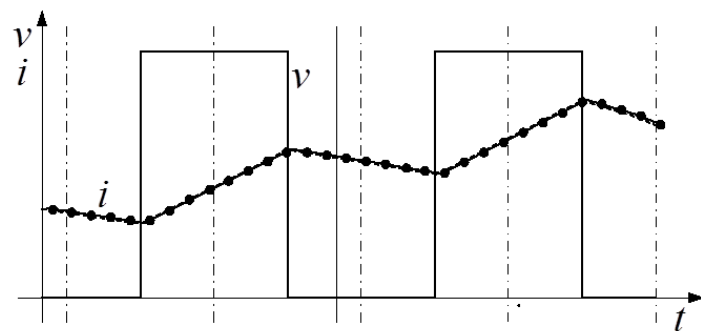


Figure 7. Sampling strategies for capturing multiphase control signals: synchronous sampling with a low frequency (upper graph) or asynchronous oversampling (lower graph).

mechanical components that the motor drives or moves to consider their behavior (such as the backlash of gear wheels) in the test.

Typical disadvantages of the simulation at the mechanical level are the effort required for the test setup, the costs, which are higher in comparison with simulation at the power level, and the relatively complex infrastructure required by the mechanical test bench. Furthermore, such test setups are not flexible because testing different motors entails a great effort.

Another general challenge is the precise digital capture of the drive's multiphase PWM control signals, the position sensor simulation, and fast simulation models of the electric components. Dynamic, high-precision drives require the real-time computation and output of signals several times in each PWM period.

Additional challenges are caused by the requirement to display nonlinear effects of the power electronics components in the real-time simulation. Today's ECUs for electric motors already take nonlinear effects such as cogging torque and magnetic saturation in the stator into account.

This shows that the control strategies of electric drive ECUs are becoming more important. This is why exact simulation of e-drive behavior in real-time applications is necessary to investigate the performance of the control loop.

E. Sampling Strategies

A general challenge for the HIL simulation of electric drives is the precise digital capture of the drive's multiphase PWM control signals and the associated simulation of position sensor signals. This requires fast hardware to capture and output signals (I/O hardware) and to execute appropriate real-time models. Add to this the fast calculation of real-time models of the simulated drive components described in Section 3.

There are two basic ways for an ECU to capture PWM control signals: The signals are either sampled synchronously to the PWM signal or oversampled asynchronously (Figure 7).

The upper graph in Figure 7 shows the rectangular course of the PWM control signal for the synchronous sampling and the resulting current at inductive load. The current increases continuously when the voltage is set to high potential and decreases when the voltage is set to low potential. In the illustrated case, the signal is sampled twice per period.

The ECU measures the motor current resulting from this PWM control signal. This is not done continuously but at fixed sample time points, usually at the pulse center.

The HIL simulator's I/O board measures and integrates the control voltage between two sample points. The motor model uses this voltage-time area to calculate a mean current (mean value model) and outputs it before the following sample point. The current is output with a lag of one sample time point. This can usually be tolerated.

This kind of low-rate synchronous sampling requires that the measurement of the PWM pulse widths and the calculation of the motor model are executed synchronously to the PWM period to avoid subharmonic frequencies. In this approach for the real-time simulation of electric motors, which has been established for years, the output signals are often updated only once during a PWM cycle (or with a small multiple).

But the requirements for developing the dynamic, high-precision ECUs of electric drives can exceed the capabilities of low-rate synchronous sampling. For a further developed HIL simulation, the signals have to be calculated and output more often during one PWM period (see lower graph in Figure 7). Here, subharmonic frequencies can be neglected, even without synchronization.

V. Real-Time Simulation

To perform a HIL test of the e-motor ECUs, I/O models and precise models of the electric motor have to be calculated in real time with small model step sizes.

Both normal processors and FPGAs are used to calculate the real-time models. At least some of the real-time models are executed on the processors to achieve a particularly small model step size.

This section describes processor-based simulation and FPGA-based simulation.

A. Processor-based Simulation

Figure 8 shows a block diagram of the hardware for the processor-based simulation of electric motors for simulation at signal level. In this case, the plant models for the power stage, the electric motor, and the mechanics are calculated on the real-time processor.

In processor-based simulation, control loops are usually calculated with a maximum frequency of 20 kHz, synchronously to the PWM control frequency (see Section 2.4). This upper limit is defined by the cycle time required by the real-time models and by the latency between the capture and output of the I/O signals.

During the synchronous sampling of the PWM control signal once per PWM period, the fast changing parts of the plant model (in this case a mean value model) are calculated within a task with a maximum cycle time of 50 μ s. During this time, the plant models of the power stage and the electric motor (without the transmission and other mechanical components) are calculated, the center-aligned PWM signal measurement takes place and the calculated current is output (see upper graph in Figure 7). Model parts that simulate the less dynamic processes of mechanical components that are connected to the motor can be calculated with a longer cycle time. Here, a cycle time of 1 ms is common.

Interfaces optimized for the individual signals are crucial for the simulation of electric motors with low-rate synchronous sampling. The most important requirement is an exact center-aligned measurement of PWM control signals. This requires a resolution far below 1 μ s.

Measuring the control signals of a B6 bridge requires capturing the running time of the high-side and low-side drivers, the dead time between the two drivers, and the PWM cycle time for each of the three phases. This requires specific I/O boards.

Synchronously to the PWM signal, the I/O boards have to generate interrupts which trigger the calculation of the mean value model. These interrupts are center-aligned to the PWM signal.

The simulation of current and position sensors does not require specific I/O boards. However, a specific I/O board becomes necessary when digital encoders or resolvers with high-frequency signals have to be simulated.

Usually, FPGA-based I/O boards are used for these tasks.

B. FPGA-based Simulation

The processor-based simulation of electric machines described in the previous section cannot be used for the oversampling described in this section, because the processing speed of common processors is too slow and there is no communication between the I/O boards and the real-time processor.

These limitations are overcome by FPGA-based simulation, which calculates the model parts requiring a calculation with short cycle times in an FPGA directly on the I/O board. Figure 9 shows a block diagram of the hardware for the FPGA-based simulation of electric motors at signal level.

The latency between capturing and outputting values is reduced from 25...30 μ s to approx. 1 μ s compared with the usual mean value models, and the simulated current values can be output at intervals of 100 ns.

With such a high-resolution simulation it is possible to simulate the PWM-induced current ripple in inductances, improve the precision of the simulation at high PWM frequencies, and represent the closed control loops with a HIL simulator exactly and stably. In addition, the FPGA-based simulation also makes it easier to emulate nonlinear effects of the power electronics components in real time.

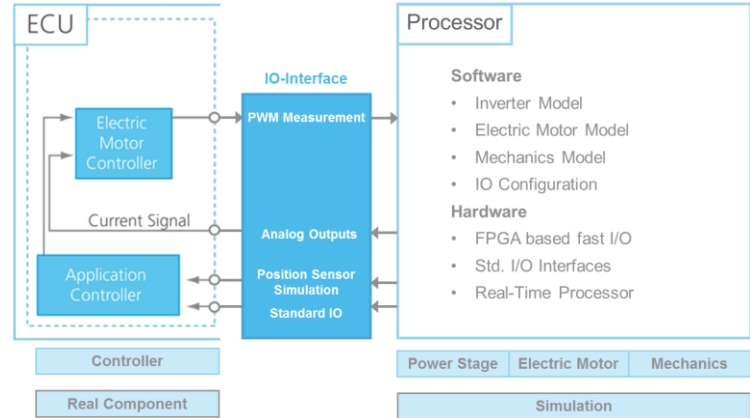


Figure 8. Processor-based simulation of electric motors.

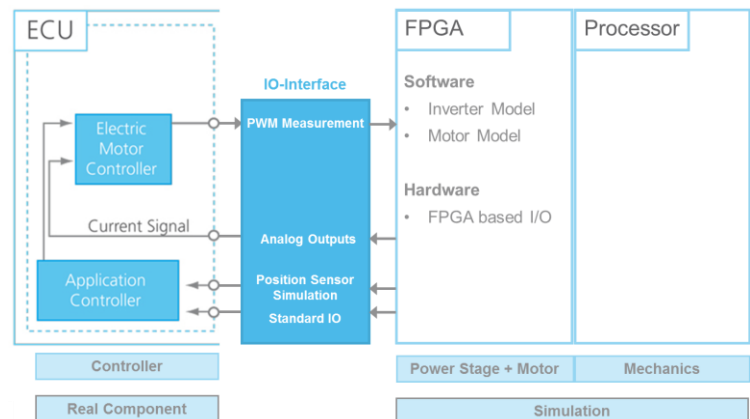


Figure 9. FPGA-based simulation of electric motors.

Figure 10 shows an example for the simulation of current ripples: the current behavior in the stator of a permanent magnet synchronous motor with a torque of 6250 rpm; the PWM frequency is 32 kHz.

VI. HIL Simulation

The development of sophisticated power electronics requires a flexible HIL test system with powerful FPGA technology connected to the processor. The system must also provide a convenient library for modeling electrical components.

FPGA technology has to be included because electric drives require the simultaneous computation of complex simulation models in real time and high-precision measurement of the ECU signals. Generally, it is often time-critical I/O computations that are described by an FPGA model. Even parts of the plant model are frequently executed on the FPGA.

Additional requirements occur due to the number of I/O channels and the need for a low-latency connection between the FPGA board and the real-time processor. Extensive system setups can easily require an extremely large number of I/O channels, so a low-latency, high-bandwidth (up to 100 MB/s) connection is needed. The I/O signals also have to be updated on the ECU according to the specified model step size. Only extremely powerful HIL network technology can fulfill these preconditions.

In the following subsection, the HIL technology SCALEXIO [1] is used as an example to present the simulation at signal level, power level, and mechanical level. SCALEXIO uses the I/O network IOCNET, which is used for high bandwidths and low latencies and supports the required model synchronization on the real-time processor and the FPGA.

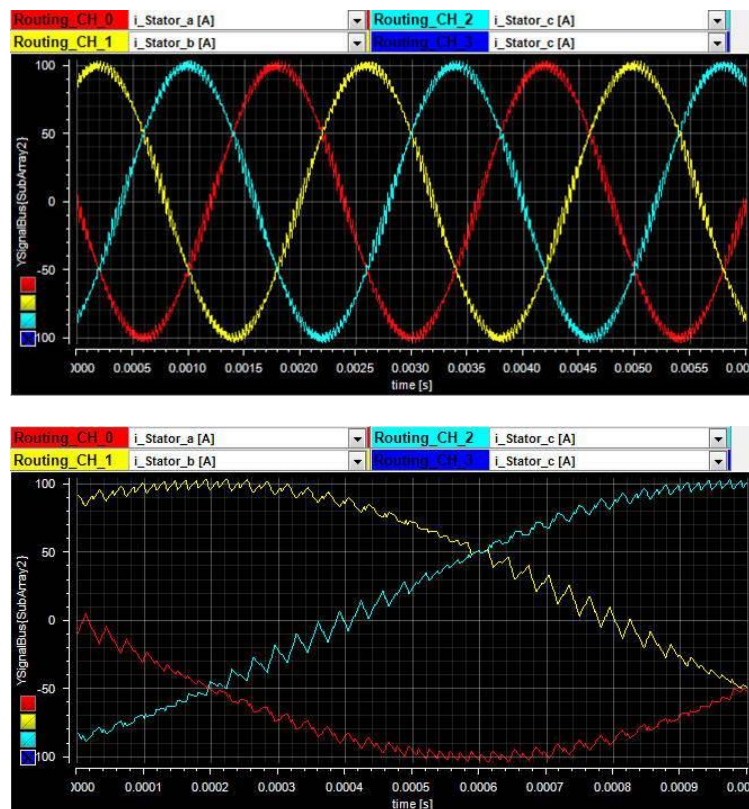


Figure 10. Simulation of the current ripples of a permanent magnet synchronous motor.

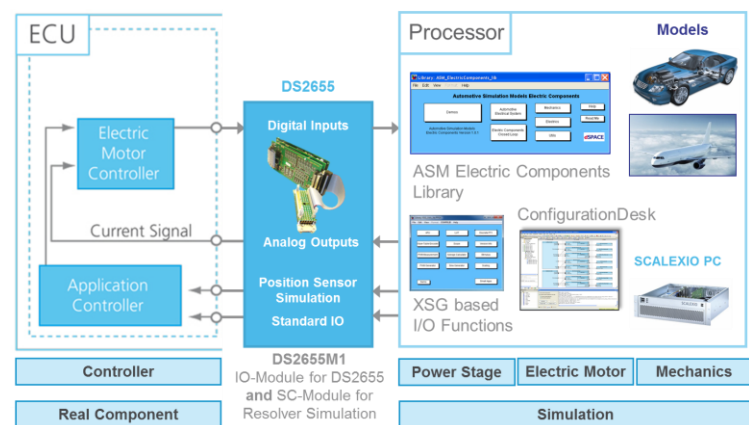


Figure 11. Processor-based simulation at signal level.

A. Signal Level

Figure 11 and Figure 12 illustrate the hardware and software components for processor-based simulation and FPGA-based simulation at signal level.

A comparison of the two figures shows that the same simulator hardware is used. Both examples use the same FPGA I/O board, which is connected to the SCALEXIO real-time PC via the fast, serial I/O network IOCNET.

In both cases, we use the same tool, ConfigurationDesk, to configure the HIL simulator and implement the real-time application.

For processor-based simulation, Simulink models (in this case, from the open ASM Electric Components Library) of the electrical components are calculated on the SCALEXIO PC. The I/O models for the digital input signals (PWM measurement), the analog current output signals, the simulation of the position sensors, and the

standard I/O are executed on the FPGA board (freely programmable DS2655 FPGA Base Board with associated DS2655M1 I/O Module).

In FPGA-based simulation, which enables oversampling, FPGA models instead of Simulink models are used for the electrical components. In this example, these models are taken from the XSG Electric Components Library. This open library contains components that are needed for the simulation of electric motors, such as a permanent magnet synchronous motor, various direct current motors, different incremental encoders, and help functions such as mean value calculation, look-up tables, or center-aligned PWM measurement.

During the simulation, there has to be data exchange between Simulink models on the real-time processor and the fast models in the FPGA, so that the models can be parameterized and the model data of the FPGA model can be visualized. In addition, easy access to the I/O of the FPGA board is necessary on a level of abstraction. An interface between the Simulink and FPGA model fulfills these two requirements and is represented schematically in Figure 12.

This interface is generated partly automatically to allow easy handling. The user does not require special FPGA programming skills but only needs some experience in working with Simulink and hardware. Figure 13 shows an example of the automatic interface generation.

B. Power Level

Figure 14 shows the hardware and software components for FPGA-based simulation at power level. The same FPGA I/O module is used as in the SCALEXIO simulator technology presented in Figure 12. In contrast to the simulation at signal level, the ECU's power stages are included in the test. This means that real currents for the ECU interfaces and the load of these interfaces have to be generated, depending on the operating point.

The state-of-the-art technology for emulating motor currents is active, highly dynamic electronic load modules that function as both current source and sink to provide a bidirectional current flow.

The load module for three-phase motor control in Figure 14 uses power recovery to drastically reduce current losses. This is an integral prerequisite for testing powerful drives. This module has a working range of up to 60 V and 10 A. Higher voltages can be covered by switching several modules in parallel.

Typical applications in the automotive field include starter-generator systems, mild hybrids, and electronic power steering.

For higher-voltage drives, there are load emulators that cover voltages of up to 800 V and output powers of up to 100 kW.

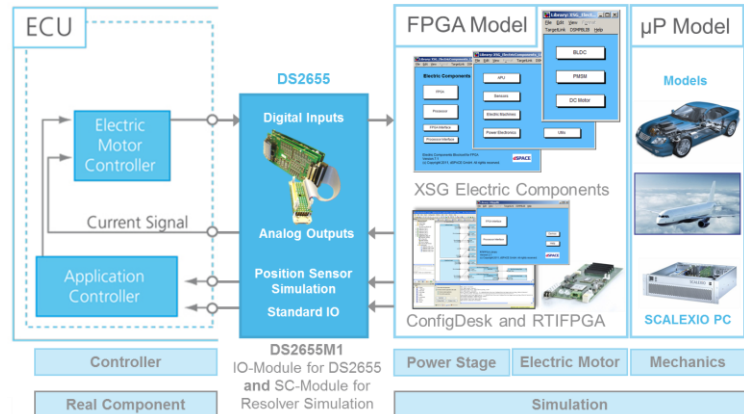


Figure 12. FPGA-based simulation at signal level.

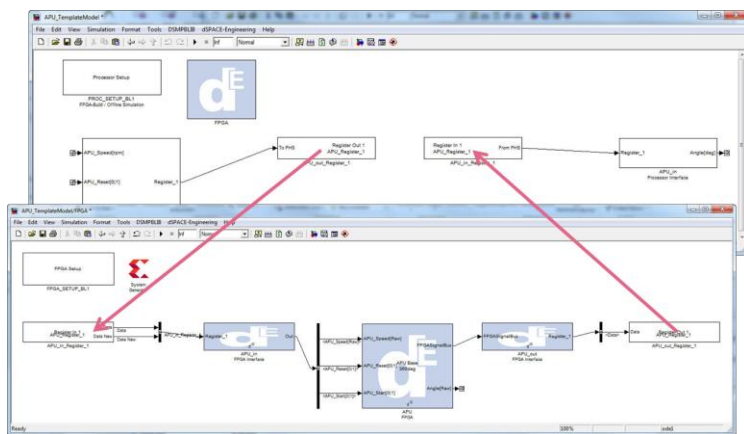


Figure 13. FPGA-based simulation at signal level.

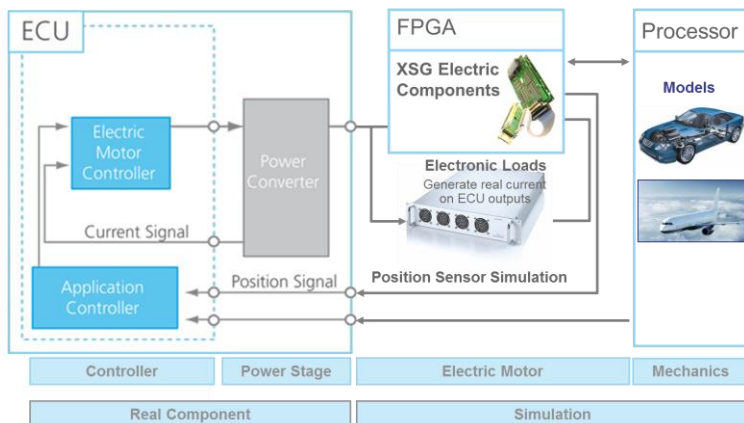


Figure 14. FPGA-based simulation at the power level.

C. Mechanical Level

Figure 15 is a schematic of the processor-based simulation at the mechanical level. Such test benches enable testing large integrated drives, considering mechanical effects in the test and, if applicable, testing the mechanical limits of the drive.

Testing at the mechanical level requires a low latency between the real-time models on the HIL simulator and the test bench and the control of a highly dynamic load machine by the HIL simulator.

In the automotive industry, testing at the mechanical level is widely used.

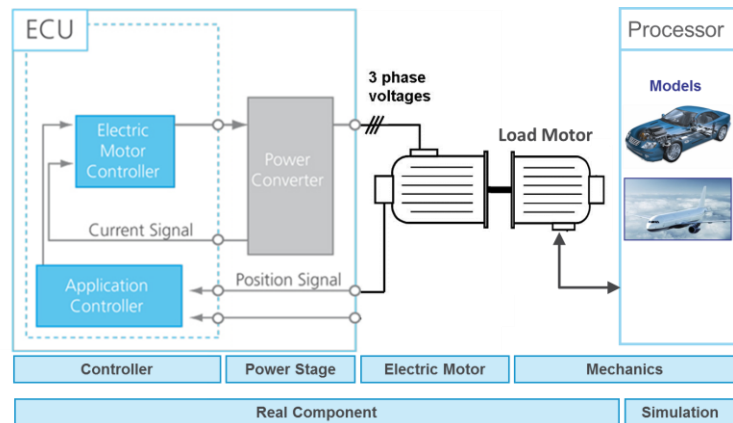


Figure 15. Processor-based simulation at the mechanical level.

VII. Summary

This article describes the state of the technology for the HIL simulation of electric drives. First, the characteristics and challenges of the simulation at the signal level, power level, and mechanical level are described, as well as the sampling strategies of the PWM control signals, the standard low-frequency synchronous sampling and the asynchronous oversampling. The article also describes how using I/O boards in FPGA-based simulation helps meet the time requirements for the model calculation. Building on the first sections, a state-of-the-art HIL technology is used to identify the hardware and software that is currently available and being used for HIL simulators for the observed simulation levels.

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